Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1.-3. Cancelled.

4. (Currently amended) A circuit comprising:

a first delay device including a control input and at least one output;

a second delay device including a control input and at least one output;

a control signal line coupled to, and configured to provide a control signal to, the control input of the first delay device and the control input of the second delay device, the control signal being based on an output of the first delay device and on a clock;

a sampling signal line coupled to, and configured to provide a sampling signal based on, an output of the first delay device; and

a sampling device coupled to an output of the second delay device and coupled to the sampling signal line, the sampling device configured to sample the output of the second delay device based on a value of the sampling signal,

wherein the second delay device includes multiple outputs, and the sampling device is coupled to the multiple outputs.

5. (Previously presented) The circuit of claim 4 further comprising a comparator that includes a first input coupled to an output of the first delay device, a second input coupled to the clock, and an output coupled to the control signal line.

6. (Previously presented) The circuit of claim 5 wherein the comparator is configured to provide on the output an error signal between the output of the first delay device and the clock.

7. (Previously presented) The circuit of claim 6 further comprising a voltage adjustment device disposed between the output of the comparator and the control signal line, and configured to provide the control signal on the control signal line based on the error signal.

8. (Previously presented) The circuit of claim 4 wherein the first delay device includes multiple outputs, the sampling signal line is coupled to the multiple outputs, and the sampling signal is based on the multiple outputs.

9. (Previously presented) The circuit of claim 8 wherein the multiple outputs include a first output and a second output and the circuit further comprises an exclusive-OR device, the exclusive-OR device including (i) a first input coupled to the first output of the first delay device, (ii) a second input coupled to the second output of the first delay device, and (iii) an output coupled to the sampling signal line.

10. Cancelled.

11. (Currently amended) The circuit of claim ~~10~~ 4 wherein the sampling device comprises a latch configured to sample the multiple outputs together based on the value of the sampling signal.

12. (Previously presented) The circuit of claim 4 wherein the sampling device comprises a latch.

13. (Previously presented) The circuit of claim 4 wherein the first delay device comprises a first delay line.

14. (Previously presented) The circuit of claim 13 wherein the second delay device comprises a second delay line.

15. (Previously presented) The circuit of claim 13 wherein the first delay line includes cascaded inverters.

16. (Previously presented) The circuit of claim 15 wherein the cascaded inverters include an odd number of inverters.

17. (Previously presented) The circuit of claim 15 wherein the cascaded inverters are arranged in a feedback configuration and at least two consecutive inverters are configured with common initial conditions so as to produce a distinctive pattern during operation of the first delay line.

18. (Previously presented) The circuit of claim 15 wherein the control input of the first delay line comprises a supply voltage input, and a level of supply voltage on the supply voltage input affects switching speed of the cascaded inverters.

19. (Previously presented) The circuit of claim 14 wherein the second delay line comprises an input configured to be coupled to a data source and is configured to hold data representing one bit of the data source.

20. (Previously presented) The circuit of claim 19 wherein the sampling device is configured to sample the data with multiple samples such that each bit is sampled multiple times.

21. (Previously presented) The circuit of claim 4 wherein the second delay device comprises an input configured to be coupled to a data source.

22. (Previously presented) A circuit comprising:

a first delay line including an odd number of cascaded inverters, a supply voltage input, and at least one output, the cascaded inverters being arranged in a feedback configuration and at least two consecutive inverters being configured with common initial conditions so as to produce a distinctive pattern during operation of the first delay line, wherein a level of supply voltage on the supply voltage input affects switching speed of the cascaded inverters;

a second delay line including an input configured to be coupled to a data source, multiple outputs, and a control input;

a comparator including a first input coupled to an output of the first delay line, a second input coupled to a clock, and an output, the comparator being configured to provide on the output an error signal between the output of the first delay line and the clock;

a control signal line coupled to the output of the comparator, the supply voltage input of the first delay line, and the control input of the second delay line, the control signal line being configured to provide a control signal, based on the error signal, to the supply voltage input of the first delay line and the control input of the second delay line;

a sampling signal line coupled to, and configured to provide a sampling signal based on, an output of the first delay line; and

a sampling device coupled to the multiple outputs of the second delay line and coupled to the sampling signal line, the sampling device configured to sample the multiple outputs of the second delay line based on a value of the sampling signal.

23. (Previously presented) The circuit of claim 22 wherein:

the second delay line comprises an odd number of cascaded inverters,

the control input comprises a supply voltage input, and

a level of supply voltage on the supply voltage input of the second delay line affects switching speed of the cascaded inverters of the second delay line.